

Most applications for currents of some 10A use transistors with silicon chips that are integrated in *potential-free power modules*. These modules contain one or several transistor systems, diodes adapted to the transistors (free-wheeling diodes) and, if required, passive components and „intelligence“, see chapter 1.4..1.6.

Despite the disadvantage of one-side cooling, power modules are maintaining their hold in high-power electronics against the meanwhile also available disc-cells with IGBTs and diodes, which are able to dissipate about 30 % more of the heat losses by two-side cooling. This is mainly due to „integrated“, tested *isolation* of the chips to the heatsink, possible *combinations of different components in one module* and *low costs* due to batch production, apart from their *easy assembly*.

IGBT-modules especially, are going through a permanently successful process of market penetration accompanied by increased efficiency, withstanding the new and further development of other - competitive - power semiconductors. Today IGBT-modules are produced managing a forward blocking voltage of 6.5 kV, 4.5 kV, 3.3 kV and 2.5 kV, e.g. 3.3 kV/2.4 kA [192], [196]. IGBT converters (multi-level-switch and IGBTs in series connection) for the MW-range up to more than 6 kV supply voltage can already be produced now . MOSFETs, on the other hand, are being developed for even higher frequency applications; also in the high current range more than 500 kHz can be produced with the corresponding wirings and assembly topologies.

Apart from the small power application range, for which chip-on-chip solutions are gaining more and more importance, IGBT and MOSFETmodules are the basic components for the integration of complete electronic and also mechatronic systems in future.

1.2 Power MOSFET and IGBT

1.2.1 Different structures and functional principles

In the following descriptions we restrict ourselves to *n-channel-enhancement power MOSFETs and IGBTs (enhancement transistors)*, representing the majority of transistors used in power modules.

If a *positive control voltage* is applied, a *conducting channel with electrons as charge carriers* (majority carriers) is generated within the existing *p-conducting silicon*. Without applying a control voltage, these components would block (self-blocking).

Other designs, which will not be dealt with any further in this chapter, are *p-channel-enhancement transistors* (induction of a positively charged channel within p-silicon by applying negative control voltage/self-blocking) and *n- and p-channel depletion types (depletion transistors)*, which turn on without applied control voltage (self-conducting). In these transistors, the control voltage generates a space charge zone that cuts off the channel and interrupts the main current flow.

In most applications the *vertical structures* shown in Figure 1.2 and Figure 1.4 are used, where gate and source (MOSFET) or emitter (IGBT) are located on top of the chip, whereas the chip bottom serves as drain (MOSFET) or collector connection. The load current is conducted vertically through the chip outside the channel.

The power MOSFETs and IGBTs shown in the sections have a *planar gate structure*, i.e. a *lateral* (horizontal) conductive channel is generated in case of on-state.

The *planar gate*, which has been further developed to the *double-implanted gate* in modern *high-density* transistors, is the dominating gate structure for power MOSFETs and IGBTs still today.

However, recently developed transistors have a *trench-gate-structure*, with the gates integrated vertically to the structure. During on-state, a *vertical channel* is generated on both sides of the gate. These and other new developments not dealt with any further in this chapter will be discussed in chapter 1.2.4.

The *lateral* MOSFET- and IGBT-structures taken over from microelectronics also have their drain- or collector layer allocated on their chip surface as n⁺-(MOSFET) or p⁺-well. Load current is conducted horizontally through the chip. Since the n-zone can be isolated to the IC-substrate by an oxide layer, several isolated MOSFETs or IGBTs may be integrated together with other structures on one chip.

Due to the fact that lateral transistors are only able to generate a current density of about 30 % of that in vertical structures and, thus, require more space on the assembly, they are used preferably in complex, monolithic circuits.

The structural design of the power MOSFET (Figure 1.2) as well as the IGBT (Figure 1.4) consists of a silicon-micro-cellular structure of up to 820,000 cells per cm² (latest high-tech 60 V-MOSFETs) or about 100,000 cells per cm² (high-voltage-IGBTs) distributed over a chip surface of 0.3...1.5 cm².

The cell-sections show the analogue structure of the MOSFET and IGBT control zones.

The n⁻-zone has to take up the space charge zone during off-state and accommodates p-charged wells with a low marginal (p⁻) and a high central (p⁺) doping.

These wells also include n⁺-silicon-layers which are connected to the aluminium- metallized source (MOSFET) or emitter (IGBT) electrode. A control zone (gate) consisting, for example, of n⁺-polysilicon is embedded in a thin isolation layer of SiO₂ above the n⁺-areas.

By applying a sufficient positive control voltage between gate and source (MOSFET) or emitter (IGBT), an inversion layer (n-conducting channel) is generated in the p-area below the gate. Electrons may be conducted from source or emitter to the n⁻-drift-area via this channel.

In contrast to the identical structure of MOSFET and IGBT including the n⁻-zone, there are differences regarding the third electrode, which will determine all further functions.

Power-MOSFET [277]

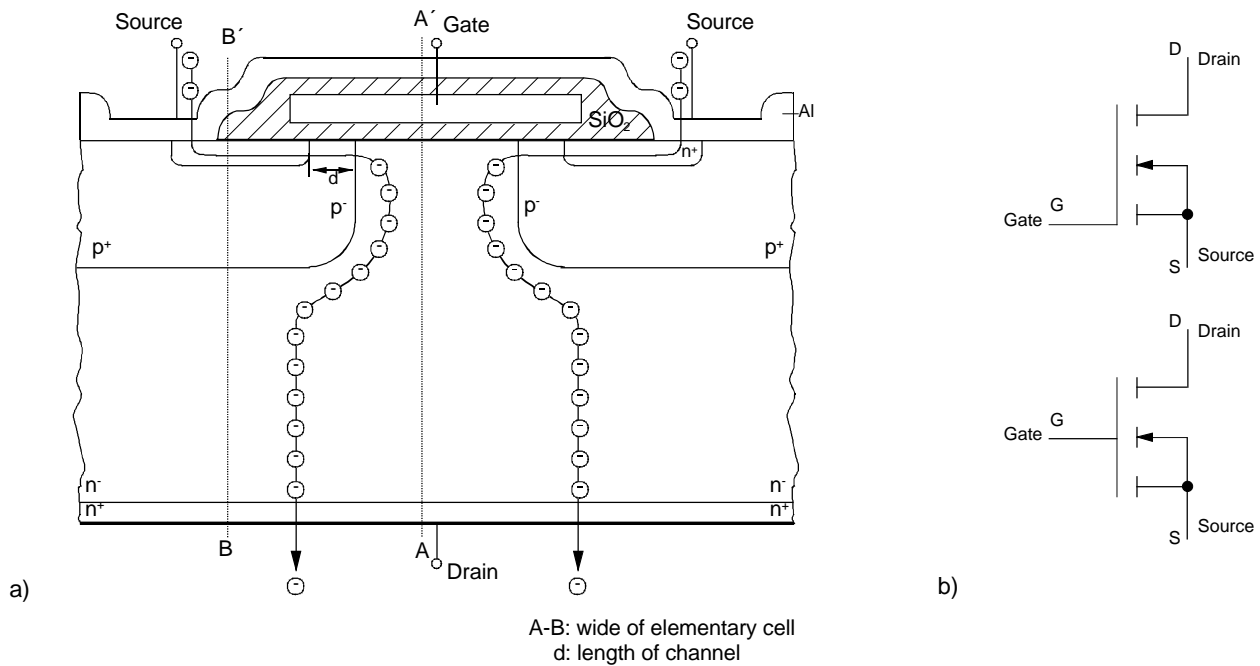


Figure 1.2 Power-MOSFET (SIPMOS Siemens)
a) MOSFET-cell with charge flow during on-state
b) Common switch symbols

Figure 1.2 explains the structure and function of a *vertical n-channel-enhancement* power-MOSFET with *planar* gate structure.

The MOSFET's layer structure described above results from epitaxial, implantation and diffusion processes on a substrate of n^+ -conductive silicon material with a drain contact on its reverse side.

The electrons flowing in the electrical voltage field between drain and source are attracted by the drain connection, thus absorbing the space charge zone; consequently, the drain-source voltage will decrease and the main current (drain current) will be able to flow.

Since the electrons are conducting current by 100 % and are majority charge carriers in the n^- -drift area, the highly resistive n^- -zone will not be flooded by bipolar charge carriers; the MOSFET is a *unipolar* component.

Whereas the drain-source on-resistance of low-voltage MOSFETs is composed of single cellular resistances about 5 % to 30 %, 95 % of the $R_{DS(on)}$ of high reverse voltage MOSFETs result from the n^- -epitaxial area resistance.

Therefore, on-state voltage drop

$$V_{DS(on)} = I_D \cdot R_{DS(on)} \quad \text{with } I_D: \quad \text{drain current and}$$

$$R_{DS(on)} = k \cdot V_{(BR)DS}^{2.4...2.6} \quad \text{with } k: \quad \text{material constant, e.g. } k = 8.3 \cdot 10^{-9} \text{ A}^{-1} \\ \text{for a chip surface of } 1 \text{ cm}^2; \\ V_{(BR)DS}: \quad \text{Drain-source forward breakdown voltage}$$

as a theoretical limit value of the actually available MOSFETs is always higher for MOSFETs from about 200...400 V off-state voltage than for comparable bipolar components and the current

carrying capacity is lower. Recently developed structures with improved parameters will be dealt with in chapter 1.2.4.

On the other hand, there are no storage effects because the majority charge carriers are exclusively responsible for charge transportation. Very short switching times may be produced however, requiring rather high control currents for changing the internal capacitances in the case of extensive components (high voltage/ high current) with about $0.3 \mu\text{C per cm}^2$ chip surface.

The capacitances resulting from the physical structure of the MOSFETs are the most important parasitic elements in Figure 1.3; their influence on the characteristics of components will be described in the corresponding chapters.

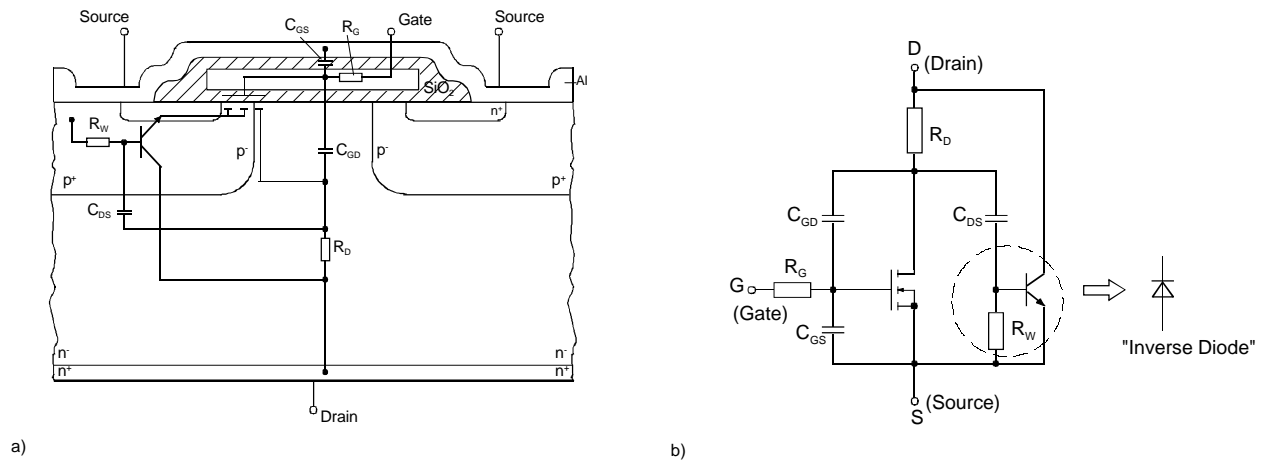


Figure 1.3 Power-MOSFET-cell with the most important parasitic elements
a) Parasitic elements within the cellular structure
b) Equivalent circuit with parasitic elements

The following table explains causes and designations of the parasitic capacitances and resistances in Figure 1.3:

Symbol	Designation	
C_{GS}	Gate-source capacitance	Overlapping gate and source metallization; dependent on gate-source voltage; independent of drain-source voltage
C_{DS}	Drain-source capacitance	Junction capacitance between n^- -drift zone and p-well; dependent on cell surface, drain-source breakdown voltage and drain-source voltage
C_{GD}	Gate-drain capacitance	Miller capacitance; generated by overlapping of gate and n^- -drift zone
R_G	Gate resistance (internal)	Poly-silicon-gate resistance; in modules with several transistor chips often additional series resistors are needed to minimize oscillations between chips
R_D	Drain resistance	Resistance of n^- -zone; often main part of MOSFET- <i>on-state-resistance</i>
R_W	Lateral resistance of p-well	Base-emitter resistance of parasitic npn- bipolar transistor

Storage charge enhancement and depletion processes cause switching losses, a delay time (storage time) and a collector tail-current during turn-off. (see chapter 1.2.3).

Apart from the "Non-Punch-Through"-structure (NPT) shown in Figure 1.3, the "Punch-Through" (PT)-structure is also applied in IGBTs today. It was the conceptional basis for the first IGBTs.

Basically, the two structures differ in the PT-IGBT's highly-doped n^+ -layer (buffer layer) between n^- - and p^+ -zone and in the manufacturing process.

Whereas the n^+ - and n^- -layers in a PT-IGBT are usually generated on a p^+ -substrate by an epitaxial procedure, the basis of the NPT-IGBT is a thin, hardly doped n -wafer, at the reverse side of which the collector p^+ -zone is generated by implantation. The MOS-control zones on top of both IGBTs are identical in their planar structure.

Figure 1.5 compares both IGBT-structures and their electrical field characteristics during off-state.

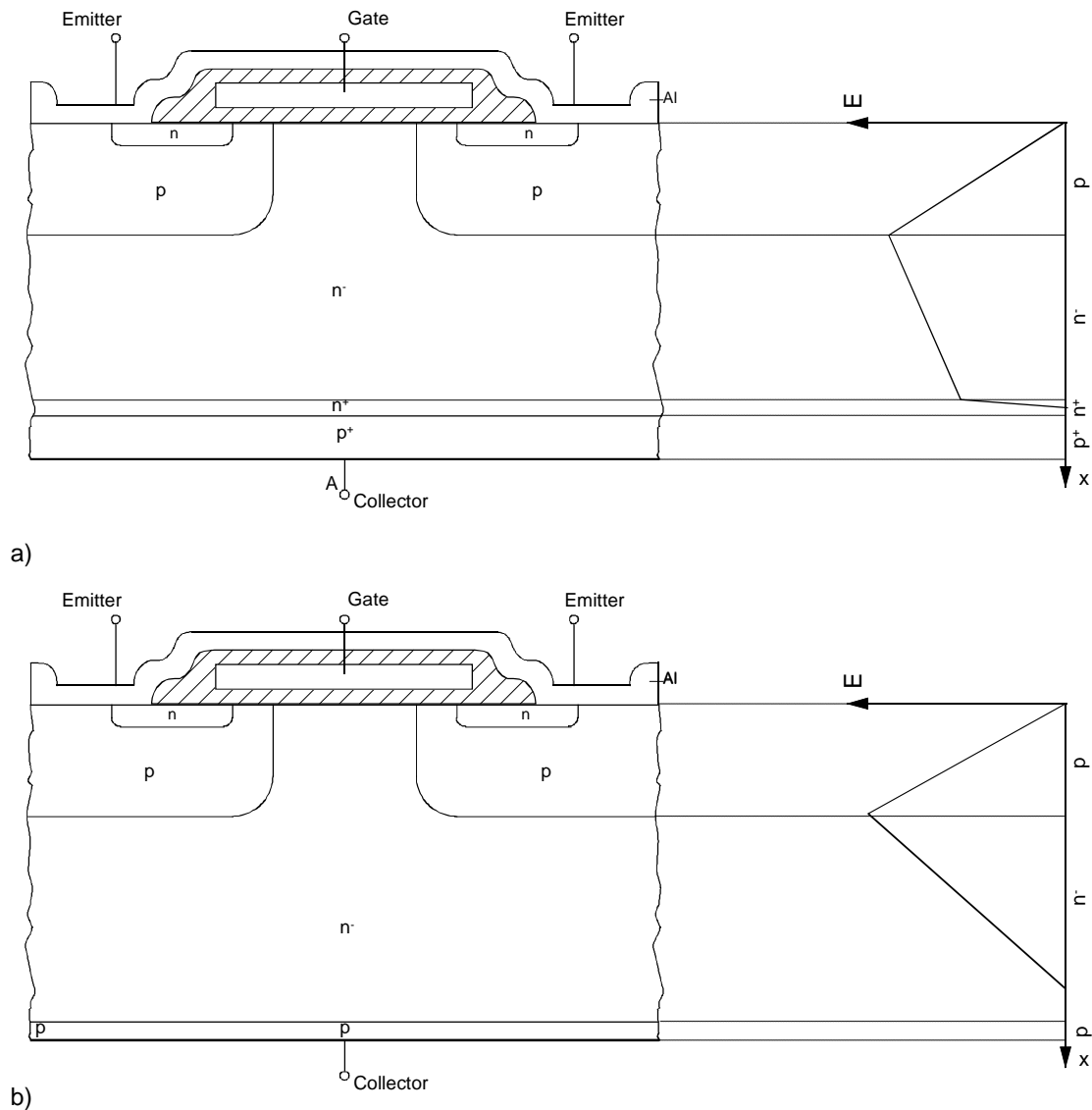


Figure 1.5 IGBT-structures and off-state electrical field characteristics [193]

- a) PT-IGBT
- b) NPT-IGBT

The space charge zone in a *PT-IGBT* or *IGET* (**E**: epitaxial structure) spreads over the whole n^- -area during off-state. In order to keep the epitaxial layer as thin as possible for high off-state voltages also, the electrical field is reduced by the highly doped n^+ -buffer at the end of the n^- -drift area.

The n^- -drift area in an *NPT-IGBT* or *IGHT* (**H**: homogeneous structure) is dimensioned large enough so that the electrical field can be completely discharged within the n^- -drift area during off-state at maximum off-state voltage. The electrical field cannot spread over the whole n^- -zone (punch through) within the permissible operation range.

For further explanations on IGBT-functions and the deviating characteristics of PT- and NPT-components it is, first of all, necessary to study the equivalent circuit resulting from the IGBT-structure (Figure 1.6b).

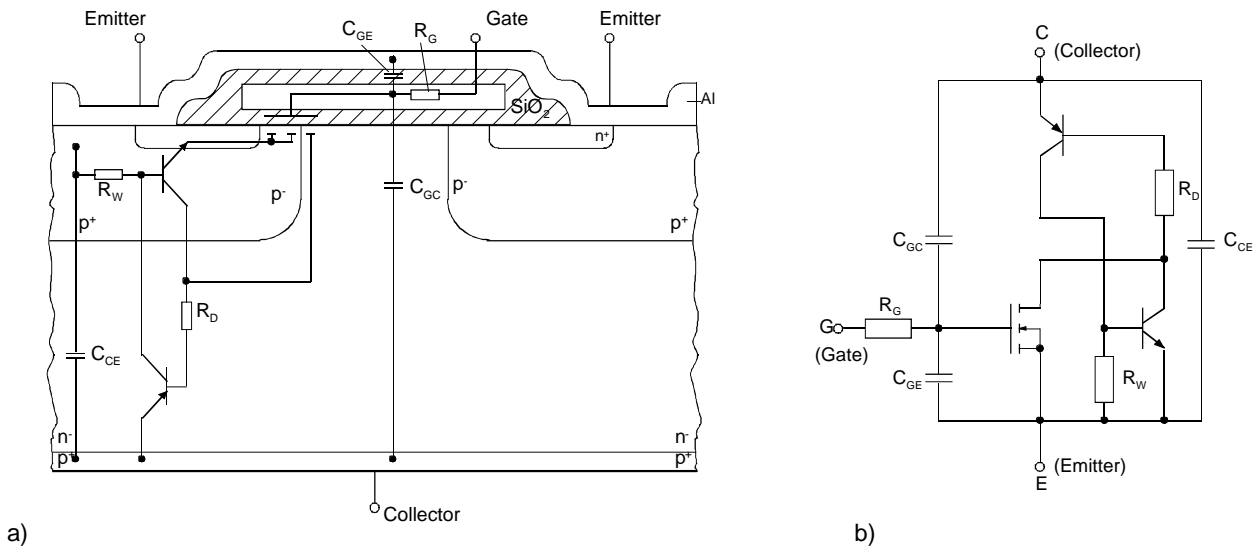


Figure 1.6 IGBT-cell (NPT-structure) with the most important parasitic elements
a) Parasitic elements in the cellular structure
b) Equivalent circuit with parasitic elements

Causes and designations of the parasitic capacitances and resistances in Figure 1.6 are analogous to Figure 1.3.

Symbol	Designation	
C_{GE}	Gate-emitter capacitance	Overlapping gate and source metallization; dependent on gate-emitter voltage; independent of collector-emitter voltage
C_{CE}	Collector-emitter capacitance	Junction capacitance between n^- -drift zone and p-well; dependent on cell surface, drain-source breakdown voltage and drain-source voltage
C_{GC}	Gate-collector capacitance	Miller-capacitance: generated by overlapping of gate and n^- -drift zone
R_G	Gate resistance (internal)	Poly-silicon-gate resistance; in modules with several transistor chips often additional series resistors are needed to minimize oscillations between chips
R_D	Drift resistance	Resistance of n^- -zone (base resistance of a pnp-transistor)

Symbol	Designation	
R_W	Lateral resistance of p-well	Base-emitter resistance of the parasitic npn-bipolar transistor

Apart from internal capacitances and resistances, the equivalent circuit of the IGBT also shows features of the „ideal MOSFET“ and the parasitic npn-transistor: n^+ -emitter zone (emitter)/ p^+ -well (base)/ n -drift zone (collector) with the lateral p^+ -well resistance below the emitters as base-emitter resistance R_W . In addition to that a pnp-transistor may be generated by sequence of p^+ -collector (emitter)/ n^- -drift (base)/ p^+ -well (collector), which represents together with the npn-transistor thyristor circuit.

Latch-up of this parasitic thyristor may happen basically during on-state (when a critical current density is exceeded, which decreases with rising chip temperature) and also during turn-off (dynamic latch-up due to the increased hole current compared to on-state operation), as soon as the following latch-up preconditions are met:

$$M \cdot (\alpha_{npn} + \alpha_{pnp}) = 1 \quad \text{with} \quad \alpha_{pnp}, \alpha_{npn} = \alpha_T \cdot \gamma_E$$

M : multiplication factor;
 $\alpha_{npn}, \alpha_{pnp}$: current gain of the single transistors in base circuit;
 α_T : base transportation factor;
 γ_E : emitter efficiency

This will lead to a loss of controllability of the IGBT and, therefore, to its destruction.

The following design measures will reliably prevent latch-up in modern IGBTs under all permissible static and dynamic operation conditions; the turn-off current density of dynamic latch-up, for example, is about 15 times the rated current density.

At first, the base-emitter resistance R_W of the npn-transistor is reduced by means of

- high doping of the p^+ -well directly below the n-emitters, and
- shortening of the n-emitters

to such an extent, that the threshold voltage of the npn-transistor base-emitter diode will not be reached in any permissible state of operation.

Furthermore, the hole current (nnp-transistor base current) is kept on a minimum level by a low current amplification in the pnp-transistor. However, switching behaviour and ruggedness have to be optimized with the on-state characteristics which also depend considerably on the pnp-transistor design.

This has been produced for PT- and NPT-IGBTs in different ways [278].

For *PT-IGBTs*, the efficiency (emitter efficiency) of hole injection of the p^+ -zone into the n^- -drift area is very high, since the substrate is very thick and highly doped. The pnp-current amplification may only be lowered with the help of the base transportation factor (n^- -drift zone, n^+ -buffer), implementing additional recombination centres (e.g. by gold doping or electron beam radiation) to reduce charge carrier life time in the n^+ -zone.

The hole current adds up to 40...45 % of the total current.

In case of *NPT-IGBTs* the p^+ -emitter zone generated at the collector by implantation is much thinner than the PT-IGBT-substrate. Therefore, the doping material concentration can be exactly dimensioned during wafer production. The very thin p^+ -layer guarantees a low emitter efficiency ($\gamma_E = 0,5$) of the pnp-transistor, so that it is not necessary to lower the base transportation factor by reducing charge carrier life time.

The hole current sums up to 20...25 % of the total current.